REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Final Office Action of December 18, 2002 has been received and contents carefully reviewed. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter in claims 27-36 and 51-55.

By this Amendment, Applicant adds new claims 56-81. In addition, Applicant amends claims 37, 38, 46, 47 and 50. Accordingly, claims 27-81 are currently pending in the present application. Reexamination and reconsideration of the application are respectfully requested.

In the Office Action, the Examiner objected to the drawings under 37 C.F.R § 1.83(a); rejected claims 37 and 50 under 35 U.S.C. § 112 ¶1; rejected claims 38-41, 45-47 and 49 under 35 U.S.C. § 102(e) as being anticipated by Yasui et al. (U.S. Patent No. 5,784,039); rejected claims 42-44 and 48 under 35 U.S.C. § 103(a) as being unpatentable over Yasui et al. in view of Applicant's Admitted Prior Art (AAPA).

Applicant respectfully submits claims 37, 38, 46, 47 and 50 are in full compliance with 35 U.S.C. § 112, first paragraph, and the objection to the drawings is now believed to be moot.

The rejections of claims 38-41, 45-47 and 49 under 35 U.S.C. § 102(e) as being anticipated by Yasui et al. and claims 42-44 and 48 under 35 U.S.C. § 103(a) as being unpatentable over Yasui et al. in view of Applicant's Admitted Prior Art are respectfully traversed and reconsideration is requested.

Claim 38 is allowable over the cited references in that claim 38 recites a combination of elements including, for example, "the gate driver outputs the first voltage on a selected gate line during the application of a data signal, wherein the second voltage is applied after the first voltage, wherein the gate driver outputs a reference potential in response to a subsequent scanning clock signal after the application of the second voltage; wherein each switching device having a gate electrode connected to the selected gate line applies the data signal to the pixel electrode in response to the first voltage; wherein each switching device having a gate electrode connected to the selected gate line turns off in response to the reference potential; and wherein the second voltage is substantially equal to a potential of the data signal." None of the cited

references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 38, and claims 39-50 which depend therefrom, are allowable over the cited references.

Claim 56 is allowable over the cited references in that claim 56 recites a combination of elements including, for example, "said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 56, and claims 57-61 and 65-70 which depend therefrom, are allowable over the cited references.

Claim 62 is allowable over the cited references in that claim 62 recites a combination of elements including, for example, "supplying the first gate voltage and the second gate voltage selectively via a switching device, to the gate lines, said switching device being controlled by the shift register, said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 62, and claims 63-64 which depend therefrom, are allowable over the cited references.

Claim 71 is allowable over the cited references in that claim 71 recites a combination of elements including, for example, "a gate driver connected to the plurality of scanning signal lines, said gate driver receiving first and second control voltages and a scanning clock signal and, in response to the scanning clock signal, successively outputting the first control voltage to the scanning signal lines to drive the scanning signal lines, wherein the switching device of each pixel responds to the first control voltage to connect the first electrode with the pixel electrode, and responds to the second control voltage to disconnect the first electrode from the pixel electrode, wherein a voltage level of the first control voltage received by the gate driver changes during a period of the scanning clock signal prior to the driver selecting a successive scanning line, and wherein the voltage level of the first control voltage turns on the switching device and

the voltage level of the first control voltage is reduced substantially to a threshold voltage level but enough to maintain an on-state of the switching device during the period of the scanning clock signal prior to the driver selecting the successive scanning line." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 71, and claims 72-75 which depend therefrom, are allowable over the cited references.

Claim 76 is allowable over the cited references in that claim 76 recites a combination of elements including, for example, "sequentially applying a first voltage to each of the plurality of scanning lines, wherein the first voltage electrically connects the plurality of contact electrodes to the plurality of pixel electrodes; and sequentially applying a second voltage to each of the plurality of scanning lines, wherein the second voltage electrically disconnects the plurality of contact electrodes from the plurality of pixel electrodes, wherein the second voltage is sequentially applied to each of the plurality of scanning lines after the application of the first voltage to each of the plurality of scanning lines but prior to the sequential application of the first voltage to another one of the plurality of scanning lines." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 76, and claims 77-81 which depend therefrom, are allowable over the cited references.

Applicant believes the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. If the Examiner deems that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number (202) 496 – 7500. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the

filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

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Version With Markings to Show Changes Made

37. (Amended) The active matrix liquid crystal display apparatus of claim 27, wherein [the reference potential]second voltage is ground.

38. (Amended) A liquid crystal display (LCD) device, comprising:

a plurality of pixels arranged in rows and columns, wherein each pixel includes a pixel electrode and a switching device having a control electrode, a first electrode, and a second electrode that is connected to the pixel electrode;

a plurality of data signal lines, each connected to first electrodes of a column;

a plurality of scanning signal lines, each connected to control electrodes of a row;

a data driver for selectively applying data signals to the data lines; and

a gate driver connected to the plurality of scanning signal lines, said gate driver receiving first and second voltages and scanning clock signals;

wherein the gate driver outputs the first voltage on a selected gate line during the application of a data signal in response to a scanning clock signal, wherein the gate driver outputs the second voltage on the selected gate line during the application of the data signal, wherein the second voltage is applied after the first voltage, wherein the gate driver outputs a reference potential in response to a subsequent scanning clock signal after the application of the second voltage ;

wherein each switching device having a gate electrode connected to the selected gate line applies the data signal to the pixel electrode in response to the first voltage;

wherein each switching device having a gate electrode connected to the selected gate line turns off in response to the [second voltage]reference potential; and

wherein the second voltage is substantially equal to a potential of the data signal.

46. (Amended) The active matrix liquid crystal display apparatus as claimed in claim 38, wherein the gate [controller]driver includes a timing controller.

47. (Amended) The active matrix liquid crystal display apparatus as claimed in claim 38, wherein the gate [controller]driver includes analog switches that are controlled by a shift register.

50. (Amended) The active matrix liquid crystal display apparatus of claim 38, wherein the [reference potential]second voltage is ground.